PLLCON PAGE 1

1 ;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

2 ;

3 ; Author : ADI - Apps www.analog.com/MicroConverter

4 ;

5 ; Date : 28 September 1999

6 ;

7 ; File : pllcon.asm

8 ;

9 ; Hardware : ADuC824

10 ;

11 ; Description : Demonstrates that the CPU can run at different

12 ; speeds determined by the CD bits in the PLLCON SFR.

13 ; 2 to the power of CD (a 3 bit number), is the divider

14 ; ratio that determines the clock frequency at which

15 ; the CPU will run.

16 ;

17 ; The program turns on and off the LED approx every

18 ; 70,000 machine cycles. With the higher frequency

19 ; (CD=0 =>fcore=12.58MHz) the LED toggles at about

20 ; 16Hz. By pressing the INT0 button the CD bit is

21 ; incremented (CD=1 =>fcore=6.3MHz) and the LED will

22 ; toggle at half the frequency as before. At the

23 ; minimum frequency (CD=7, fcore=700kHz) the LED

24 ; toggles at 0.125Hz. By pressing INT0 button again

25 ; CD rolls over to 0 again and the LED

26 ; toggles at 16Hz again.

27 ;

28 ;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

29

30 $MOD824 ; Use 8052&ADuC824 predefined symbols

31

00B4 32 LED EQU P3.4 ; P3.4 drives red LED on eval board

33

34

35 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

36 ; BEGINNING OF CODE

---- 37 CSEG

38

0000 39 ORG 0000h

40

0000 020060 41 JMP MAIN ; jump to main program

42 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

43 ; INTERRUPT VECTOR SPACE

0003 44 ORG 0003h ; (INT0 ISR)

45

0003 B2B4 46 CPL LED ; complemant LED to indicate INT0

47 ; press.

0005 7A88 48 MOV R2,#136 ; reinitialise R7 and R6 so that

0007 7B00 49 MOV R3,#256 ; after interrupt the full delay

50 ; loop is completed

51

0009 E5D7 52 MOV A, PLLCON ; Only increment CD bits of PLLCON

000B 04 53 INC A ; Rollover to PLLCON = xxxxx000b (fmax)

000C 5407 54 ANL A, #07h ; after PLLCON = xxxxx111b (fmin)

000E F5D7 55 MOV PLLCON, A ; where the x's are 1's and 0's as rqd

56

0010 32 57 RETI

58

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59 ;====================================================================

60

0060 61 ORG 0060H ; Start code at address above interrupts

0060 62 MAIN:

0060 75D700 63 MOV PLLCON, #00H

0063 D288 64 SETB IT0

0065 D2A8 65 SETB EX0 ; enable ext int INT0

66 ; (button on eval board)

0067 D2AF 67 SETB EA ; enable interrupts

68

0069 B2B4 69 BLINK: CPL LED

006B 120070 70 CALL DELAY ; wait for 70,000 machine cycles

71 ; =66ms at fmax

72 ; =8.5s at fmin

006E 80F9 73 JMP BLINK

74

75

76 ;====================================================================

0070 77 DELAY: ; This loop delays the program for 70,000

78 ; (approx) machine cycles, corresponding

79 ; to a delay of 66ms at fmax and 8.4s

80 ; at fmin

81

0070 7A88 82 MOV R2,#136 ; 136 \* 256 \* 1.907us = 66ms

0072 7B00 83 DLY1: MOV R3,#256 ;

0074 DBFE 84 DJNZ R3,$ ; sit here for 256 x 2 x machine

85 ; cycle time (=488us @ fmax)

0076 DAFA 86 DJNZ R2,DLY1 ; repeat 136 times (=66ms total @ fmax)

0078 22 87 RET

88

89 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

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91 END

VERSION 1.2h ASSEMBLY COMPLETE, 0 ERRORS FOUND

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BLINK. . . . . . . . . . . . . . C ADDR 0069H

DELAY. . . . . . . . . . . . . . C ADDR 0070H

DLY1 . . . . . . . . . . . . . . C ADDR 0072H

EA . . . . . . . . . . . . . . . B ADDR 00AFH PREDEFINED

EX0. . . . . . . . . . . . . . . B ADDR 00A8H PREDEFINED

IT0. . . . . . . . . . . . . . . B ADDR 0088H PREDEFINED

LED. . . . . . . . . . . . . . . NUMB 00B4H

MAIN . . . . . . . . . . . . . . C ADDR 0060H

P3 . . . . . . . . . . . . . . . D ADDR 00B0H PREDEFINED

PLLCON . . . . . . . . . . . . . D ADDR 00D7H PREDEFINED